



Features

- PC/104 bus compatible and board compliant.
- Can be utilized as a PC/104 module or as a stand alone circuit board.
- The CPLD Master clock can be user selected between the PC/104 bus or by an installed 50MHz oscillator.
- Selectable 3.3V or 5V I/O capability.
- 34 programmable I/O pins.
- High-drive 24mA outputs.
- Utilizes the Xilinx XC95144-15QT100 CPLD.
- Fully supported by the Xilinx free Webpack software.
- IEEE 1149.1 JTAG compliant input on board.
- Circuitry based upon the Xilinx Parallel Download Cable III incorporated directly on to the circuit board.
- Can be programmed by a straight through DB25 parallel cable connected between the RP-3200 board and the host computer.
- Can be powered through the PC/104 bus or by an external DC power source.
- Available in commercial or industrial temperature.

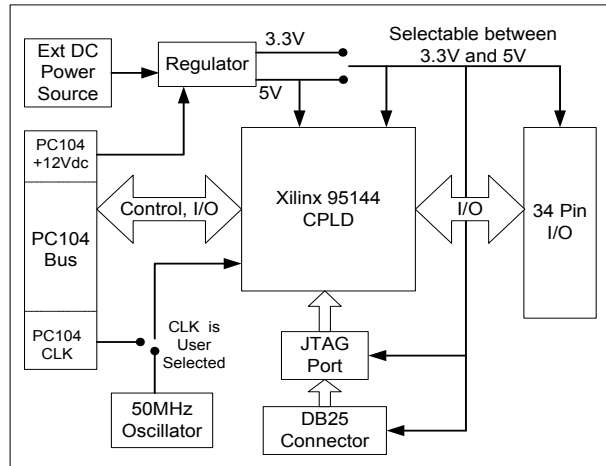
Description

The RP-3200 is a PC/104 based board featuring a Xilinx XC9500 series CPLD, integrated circuitry based upon the Xilinx Parallel Download Cable III, extensive IEEE 1149.1 (JTAG) boundary-scan support, selectable oscillator configuration and a selectable 3.3V or 5V I/O capability.

The board uses the Xilinx XC95144-15TQ100 CPLD which has extensive features including; advanced CMOS 5V FastFLASH technology, enhanced pin-locking architecture, high-drive 24mA outputs, and extended pattern security features for design protection.

The RP-3200 can be powered from the PC/104 bus or can be powered from an external DC source allowing the board to be utilized as a stacked module in PC/104 applications or as a standalone product design platform. This allows the board to be ideal in embedded

Block Diagram



Device Selection Table

Part Number	PC104 Connector Style	Temperature Range
RP-3200-NC	Non-Stackthrough	Commercial
RP-3200-SC	Stackthrough	Commercial
RP-3200-NI	Non-Stackthrough	Industrial
RP-3200-SI	Stackthrough	Industrial

PC/104 applications or to be utilized in development platforms, design prototypes or production products.

The RP-3200 allows the CPLD master clock to be manually selected from the PC/104 bus or from a 50MHz oscillator installed directly on the circuit board.

The RP-3200 has integrated circuitry based upon the Xilinx Parallel Download Cable III incorporated on the circuit board. This allows the RP-3200 to be programmed using only a straight through DB25 parallel port cable connected to a computer parallel port. In addition, the RP-3200 also has an IEEE 1149.1 JTAG port on the circuit board allowing greater programming and JTAG communications versatility.

The small size and versatility of the RP-3200 makes it a prime target for embedded applications or as an integrated part of a larger system.

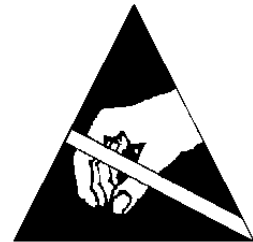
Absolute Maximum Ratings †

Symbol	Parameter	Min	Max	Units
VCCext	External supply voltage through J5 connector relative to GND	-0.5	+18	VDC
VCC-PC104	+12VDC supply voltage from the PC104 bus relative to GND	-0.5	+18	VDC
VCC-Current	Current from the J5 connector or the PC104 +12VDC supply voltage	0	1.2	ADC
V _{IN}	DC input voltage relative to GND	-0.5	+5.5 (+3.7) ¹	VDC
V _{TS}	Voltage applied to XC95144 3-state output with respect to GND	-0.5	+5.5 (+3.7) ¹	VDC
T _{STG}	Storage temperate	-50	+100	°C

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the devices. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
VCCext	External supply voltage through J5 connector relative to GND	+6.5	+14	VDC
VCC-PC104	+12VDC supply voltage from the PC104 bus relative to GND	+6.5	+14	VDC
V _{IL}	Low-level input voltage	0	+0.8	VDC
V _{IH}	High-level input voltage	2.0	+5.5 (+3.7) ¹	VDC
V _O	Output voltage	0	+5.0 (+3.3) ¹	VDC

DC Characteristics over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V _{OH}	Output High Voltage	I _{OH} = -4.0mA (-3.2mA) ¹	+2.4		VDC
V _{OL}	Output Low Voltage	I _{OL} = +24mA (+10mA) ¹		+0.5 (+0.4) ¹	VDC
I _{IL}	Input Leakage Current	V _{IN} = GND or Supply		±10	uA
I _{IH}	I/O High- Z Leakage Current	V _{IN} = GND or Supply		±10	uA

Note: 1. The first number is valid for J6 configured for 5.0VDC Operation. The second number in parenthesis is valid for J6 configured for 3.3VDC operation.

Operating Range

Range	Ambient Temperature
Commercial	0°C to +70°C
Industrial	-40°C to +85°C

Explanation of Testing

All devices are 100% tested at +25°C for functional operation. Functionality at commercial and industrial temperature extremes are validated by design.

Architecture Description

XC95144 CPLD

The RP-3200 utilizes the Xilinx XC95144-15TQ100 CPLD. The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight flexible 36V18 Function Blocks, providing 144 macrocells with 3,200 usable gates. Some of the many features of the XC95144 include: Endurance of 10,000 program/erase cycles, program/erase over full commercial temperature range, enhanced pin-locking architecture, extensive IEEE std 1149.1 boundary-scan (JTAG) support, programmable power reduction mode in each macrocell, slew rate control on individual outputs, user programmable ground pin capability, extended pattern security features for design protection, high-drive 24mA outputs, and advanced CMOS 5V FastFLASH technology.

Detailed performance characteristics, functional parameters and component limitations of the XC95144 should be referred to the XC95144 data sheet available at the Xilinx web site. (www.xilinx.com)

Power

The RP-3200 can be powered from the +12VDC supply provided in the PC104 bus or from an external power source. Internal circuitry is provided on the RP-3200 that allows power to be present on the +12VDC PC/104 and an external power source at the same time without causing any damage to the RP-3200. In this application the RP-3200 will select the higher DC voltage source to power the board. Each power source is diode protected to prevent back feeding of voltage.

The J6 connector controls predefined circuitry, external connectors and the XC95144 VCC internal supply voltage (VCC_{INT}) to be sourced by either 3.3VDC or 5VDC. The J6 connector controls the source voltage for the J8 parallel port connector and associated circuitry; J7 JTAG connector voltage and signals; the J3 source voltage; and the XC95144 VCC_{INT} . The J6 voltage selection for the XC95144 VCC_{INT} will control the voltage reference for the PC104 data bus, PC104 control signals and the J3 I/O signals.

The external power jack, J5, is a 2.1mm male jack. The center pin is positive polarity. The mating connector should be a 2.1mm female, 9.5mm long plug with positive polarity on the center pin and GND on the outside ring. **Caution:** A reverse polarity DC

signal or a AC signal applied to the J5 input power jack or pin B9 of the PC104 connector will cause damage to the RP-3200. The RP-3200 has no fuses and limited protection circuitry for the DC power source.

Care should be taken when selecting an external power source for the J5 connector or providing the power source from pin B9 of the PC104 bus for the RP-3200. The Xilinx XC95144 and the RP-3200 requires a very clean VDC source and GND reference for proper performance and programmability.

On the PC/104 connector, the +5VDC power supply pins (J1-B3, J1-B29, and J2-D16), the -5VDC power supply pin (J1-B5) and the -12VDC power supply pin (J1-B7) are not utilized nor connected on the RP-3200.

Clock Input

The XC95144 master clock input, GCLK1, can be sourced from the PC/104 CLK, (J1-B20), or from the 50MHz oscillator installed on the RP-3200, Y1. The clock source is determined by the J4 connector. Shorting pins 1 and 2 of the J4 connector will source the clock from the PC104 connector and shorting pins 2 and 3 of the J4 connector will source the clock from the installed 50MHz oscillator, Y1.

Applications requiring a unique oscillator frequency for Y1 can be preinstalled on the RP3200, contact Jacyl Technology for details.

PC104 Bus

The RP-3200 PC/104 bus is designed in a PC/104 16 bit I/O slave configuration. Only those signals required for this mode of operation are connected between the PC/104 connector and the CPLD. All signals between the PC/104 connector and CPLD are directly connected. (For a detailed listing of pin connections, refer to the section "RP-3200 Pin Definitions", "PC/104 Connector" located in this document.) The PC/104 IRQ signals incorporated on the RP-3200 are IRQ6, IRQ7, IRQ9, IRQ15, and IRQ16. This allows the RP-3200 to be programmed to control or respond to multiple IRQ priority levels from external PC/104 devices.

In the section "RP-3200 Pin definitions", "PC/104 Connector" the keyed pin locations are identified for reference only. The RP-3200 utilizes non-keyed

Architecture Description (continued)

I/O

The RP-3200 has a 40 pin male dual row header for I/O control. This connector is the J3 connector. Of the 40 pins, 34 of these pins are programmable I/O from the CPLD. The remaining 6 pins are power and GND signals that may be utilized for external circuitry. Be aware of the characteristics and limitations of each of the XC95244 I/O signals located in the J3. Refer to the Xilinx XC95144 data sheet for more detailed information.

The power signals are directly connected to the J6 selectable 3.3VDC/5VDC source allowing greater flexibility with interfacing external circuitry connected to the J3 connector. (For a detailed listing of pin assignments, refer to the section “RP-3200 Pin definitions”, “J3— I/O Connector” located in this document.)

Each of the 34 programmable I/O pins are connected to the CPLD through a 22 Ohm resistor. This 22 Ohm resistor is located in a 16 DIP package with 8 resistors in each DIP package. The 8 resistors in each 16 pin DIP packages are configured in a parallel feed through resistor network configuration. Each individual 22 Ohm resistor is rated for 0.125W @25°C. The presence and wattage of this 22 Ohm resistor needs to be kept in mind when connecting external circuitry to the J3 connector.

The current available through the power signals located in the J3 connector are directly dependent upon the current available from the external power supply or the +12VDC on the PC/104 bus and the power requirements of the XC95144.

JTAG

The RP-3200 provides two separate interfaces for programming the XC95144. A JTAG 10 pin dual row header is available on the board, J7 connector.

The RP-3200 also has circuitry based upon the Xilinx parallel Download Cable III incorporated on the board

though the J8 parallel port connector (male DB25 connector). This allows the RP-3200 to be programmed by a computer parallel port connected directly to the J8 connector by a DB25 parallel port connector. Nothing should not be connected to JTAG, J7 connector, while trying to program or communicate through the J8 parallel port connector. Failure to program or communicate with the RP-3200 could result.

The J8 circuitry, J8 signal voltage references, J7 signal voltage references and J7 supply voltage are all 3.3VDC/5VDC selectable through the J6 connector.

A high quality DB25 parallel port cable should be utilized to program and communicate with the RP-3200 through the J8 connector. It is recommended that the DB25 parallel port cable be shielded and not exceed 6' in length.

The J8 parallel port connector can only be utilized for JTAG communications and programming of the XC95144. The J8 connector contains no programmable I/O pins from the XC95144.

Programmable LEDs and Switches

The RP-3200 provides two LEDs and two switches that are connected to the CPLD. These LEDs and switches are provided as programmable visual output and selectable input to the CPLD.

The LEDs are connected through a series resistor to the J6 selectable 3.3VDC/5VDC supply.

The switches are connected to the CPLD with one side of each switch directly connected to the CPLD and pulled up to the J6 selectable 3.3VDC/5VDC voltage source through a series resistor. The other side of each switch is connected to ground.

RP-3200 Pin Definitions

PC/104 Connector

J1 Connector Pin	Signal Name	Connected to CPLD Pin
A1	IOCHCHK	N/C
A2	SD7	40
A3	SD6	42
A4	SD5	43
A5	SD4	49
A6	SD3	50
A7	SD2	52
A8	SD1	53
A9	SD0	54
A10	IOCHRDY	N/C
A11	AEN	55
A12	SA19	N/C
A13	SA18	N/C
A14	SA17	N/C
A15	SA16	60
A16	SA15	63
A17	SA14	64
A18	SA13	65
A19	SA12	66
A20	SA11	67
A21	SA10	70
A22	SA9	73
A23	SA8	77
A24	SA7	79
A25	SA6	81
A26	SA5	85
A27	SA4	87
A28	SA3	90
A29	SA2	91
A30	SA1	92
A31	SA0	93
A32	GND ⁽³⁾	—

J1 Connector Pin	Signal Name	Connected to CPLD Pin
B1	GND ⁽³⁾	—
B2	RESETDRV	40
B3	+5V ⁽²⁾	—
B4	IRQ9	46
B5	-5V ⁽²⁾	—
B6	DRQ2	N/C
B7	-12V ⁽²⁾	—
B8	ENDXFR	N/C
B9	+12V	—
B10	KEY	—
B11	SMEMW	N/C
B12	SMEMR	N/C
B13	IOW	58
B14	IOR	59
B15	DACK3	N/C
B16	DRQ3	N/C
B17	DACK1	N/C
B18	DRQ1	N/C
B19	REFRESH	N/C
B20	SYSCLK ⁽⁴⁾	22
B21	IRQ7	71
B22	IRQ6	74
B23	IRQ5	N/C
B24	IRQ4	N/C
B25	IRQ3	N/C
B26	DACK2	N/C
B27	TC	N/C
B28	BALE	N/C
B29	+5V ⁽²⁾	—
B30	OSC	N/C
B31	GND ⁽³⁾	—
B32	GND ⁽³⁾	—

Notes: 2. These PC/104 power sources are not utilized nor connected on the RP-3200.

3. GND is connected to RP-3200 GND.

4. Dependent upon pins 1 and 2 being shorted on the J4 connector.

N/C = No Connection

RP-3200 Pin Definitions (continued)
PC/104 Connector (continued)

J2 Connector Pin	Signal Name	Connected to CPLD Pin
C0	GND ⁽³⁾	—
C1	SBHE	N/C
C2	LA23	N/C
C3	LA22	N/C
C4	LA21	N/C
C5	LA20	N/C
C6	LA19	N/C
C7	LA18	N/C
C8	LA17	N/C
C9	MEMR	N/C
C10	MEMW	N/C
C11	SD8	68
C12	SD9	72
C13	SD10	76
C14	SD11	78
C15	SD12	80
C16	SD13	82
C17	SD14	86
C18	SD15	89
C19	KEY	—

J2 Connector Pin	Signal Name	Connected to CPLD Pin
D0	GND ⁽³⁾	—
D1	MEMCS16	N/C
D2	IOCS16	56
D3	IRQ10	N/C
D4	IRQ11	N/C
D5	IRQ12	N/C
D6	IRQ15	61
D7	IRQ14	N/C
D8	DACK0	N/C
D9	DRQ0	N/C
D10	DACK5	N/C
D11	DRQ5	N/C
D12	DACK6	N/C
D13	DRQ6	N/C
D14	DACK7	N/C
D15	DRQ7	N/C
D16	+5V ⁽²⁾	—
D17	MASTER	N/C
D18	GND ⁽³⁾	—
D19	GND ⁽³⁾	—

J8 —DB25 Connector

J8 Connector Pin	Signal Name
1	N/C
2	DIN
3	CLK
4	TMS_IN
5	CTRL
6	PROG
7	N/C
8	Connected to pin 11 and 12
9	N/C
10	N/C
11	Connected to pin 8 and 12
12	Connected to pin 8 and 11
13	DONE

J8 Connector Pin	Signal Name
14	N/C
15	N/C
16	N/C
17	N/C
18	N/C
19	N/C
20	GND ⁽³⁾
21	N/C
22	N/C
23	N/C
24	N/C
25	GND ⁽³⁾

N/C = No Connection

RP-3200 Pin Definitions (continued)
J3— I/O Connector

J3 Connector Pin	Pin Function	Connected to CPLD Pin
1	GND ⁽³⁾	—
2	VCC Select ⁽⁵⁾	—
3	I/O	39
4	I/O	37
5	I/O	36
6	I/O	35
7	I/O	34
8	I/O	33
9	I/O	32
10	I/O	30
11	I/O	29
12	I/O	28
13	I/O-GCK3	27
14	I/O	25
15	I/O	24
16	I/O-GCK2	23
17	GND ⁽³⁾	—
18	VCC Select ⁽⁵⁾	—
19	I/O	20
20	I/O	19
21	I/O	18
22	I/O	17
23	I/O	16
24	I/O	15
25	I/O	14
26	I/O	13
27	I/O	12
28	I/O	11
29	GND ⁽³⁾	—
30	VCC Select ⁽⁵⁾	—
31	I/O	10
32	I/O	9
33	I/O	8
34	I/O	7
35	I/O	6
36	I/O— GTS2	4
37	I/O — GTS1	3
38	I/O— GTS4	2
39	I/O— GTS3	1
40	I/O— GSR	99

J4 — CPLD Master CLK Source Selection

Pins Shorted	Function
1-2	CPLD Master CLK will be sourced from the PC104 Master CLK, J1-B20
2-3	CPLD Master CLK will be sourced from the installed 50MHz Oscillator, Y1

J6 — Voltage Reference Source Selection

Pins Shorted	Function
1-2	CPLD VCCINT, J3 (I/O) , J8 (DB25), and J7 (JTAG) will be sourced by 5VDC
2-3	CPLD VCCINT, J3 (I/O) , J8 (DB25), and J7 (JTAG) will be sourced by 3.3VDC

J7— JTAG Connector

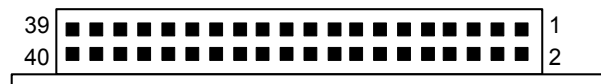
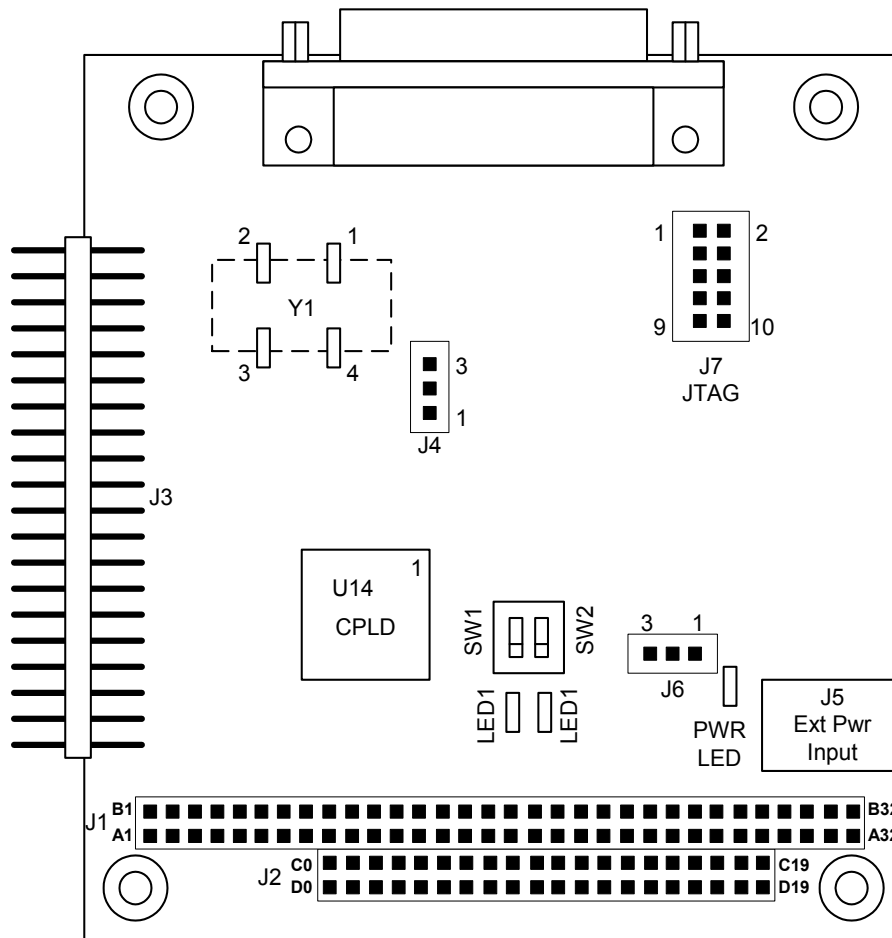
J7 Connector Pin	Signal Name
1	TDI— DIN
2	TDO— D/P
3	TCK— CLK
4	TMS— PROG
5	N/C
6	N/C
7	GND ⁽³⁾
8	VCC Select ⁽⁵⁾
9	N/C
10	N/C

RP-3200 Board Level LED and Switch Connections

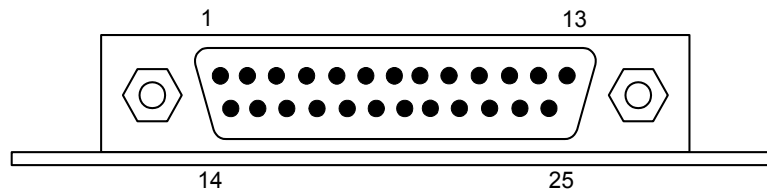
Component	Connected to CPLD Pin
LED1	96
LED2	97
SW1	94
SW2	95

Notes: 5. This voltage is dependent upon the shorting of pins 1 and 2 or pins 2 and 3 on the J6 connector.

N/C = No Connection

Connector Diagrams


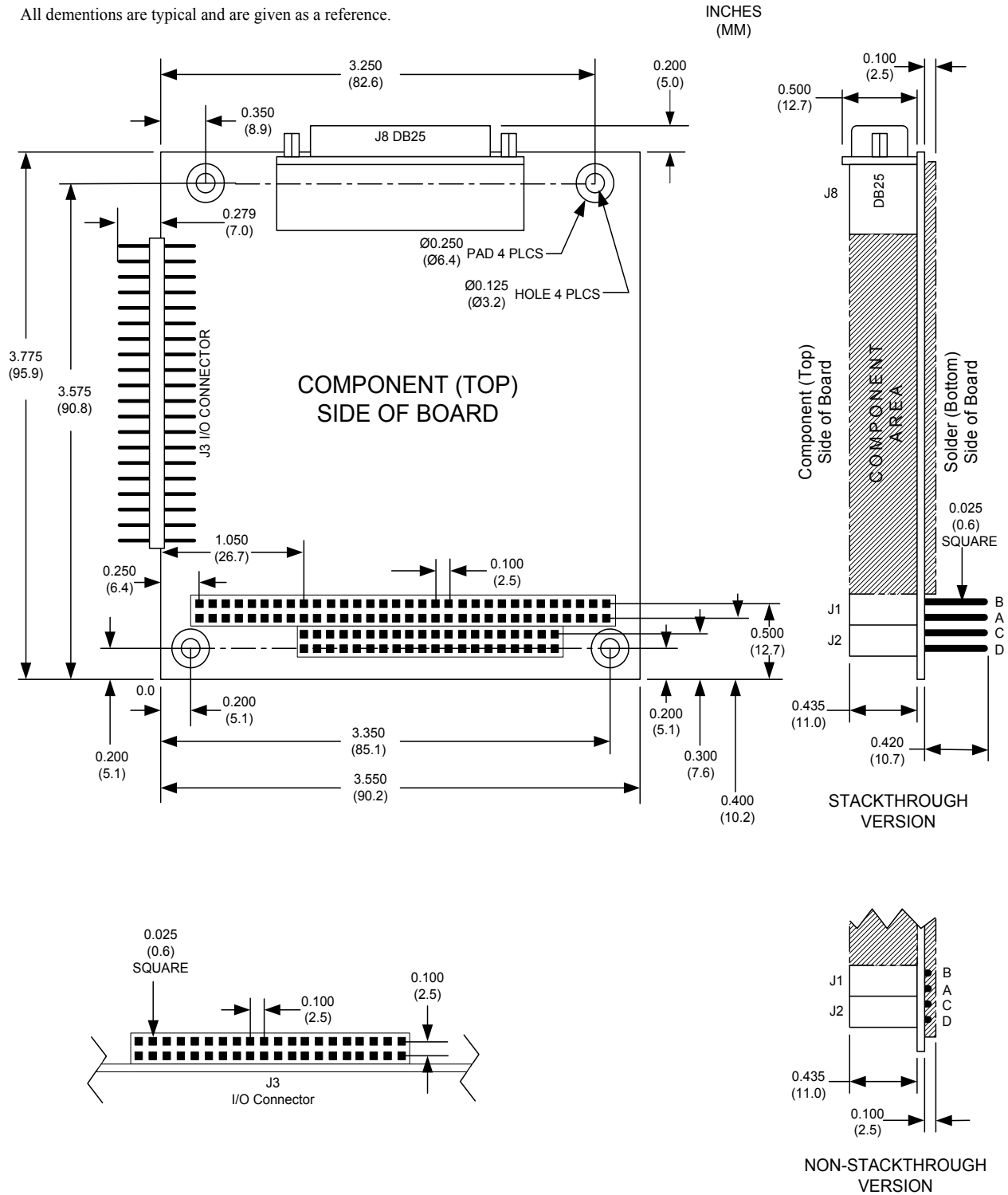
J3
I/O Connector



J8
DB25 - JTAG
Male Connector

Board Diagrams

All dementions are typical and are given as a reference.



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